

In re Patent Application of:  
**KASPER**  
Serial No. 09/163,925  
Filing Date: 09/30/1998

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transferring a burst of data after receiving a  
† start-of-packet (interrupt), including preselected address  
fields, from the FIFO receive memory to an external shared  
system memory that exists between the network device and a  
host processor;

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generating an interrupt signal to the host processor  
indicative that the preselected address fields of the frame  
are present in the shared system memory; and

initiating within the host processor an address and  
look-up algorithm in address tables to determine frame routing  
based on the preselected address fields.

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5. (ONCE AMENDED) A method of routing according  
to Claim 1, and further comprising the step of receiving a  
balance of the frame completely within the shared system  
memory.

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7. (ONCE AMENDED) A method of routing according to  
Claim 1, and further comprising the step of generating the  
start-of-packet interrupt to a communications processor within  
the network device when the data received within the FIFO  
receive memory has reached a desired watermark value.

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10. (ONCE AMENDED) A method of controlling network  
data flow arranged in frames comprising the steps of:

receiving at least a first portion of a frame  
containing data receive memory of a network device, wherein  
the first portion of the received frame includes data having  
preselected address fields;

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transferring a burst of data after receiving a start-of-packet interrupt, including preselected address fields, from the FIFO receive memory to a shared system memory that exists between a host processor and the network device; and

generating an interrupt signal to the host processor indicative that the preselected address fields of the frame are present in the memory.

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16. (ONCE AMENDED) A method according to Claim 10, and further comprising the step of generating the start-of-packet interrupt to a communications processor when the data received within the receive memory has reached a desired watermark value.

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19. (ONCE AMENDED) A method of routing network-based data arranged in frames comprising the steps of:

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receiving at least a first portion of a frame within a FIFO receive memory of a network device, wherein the first portion of the received frame includes data having preselected address fields;

selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor;

transferring a burst of data, including preselected address fields after receiving a start-of-packet interrupt, from the FIFO receive memory to a shared system memory that exists between the network device and the host processor;

generating an interrupt signal from the network device to the host processor indicative that the preselected

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address fields of the frame are present in the shared system memory; and

initiating an address and look-up algorithm to determine frame routing based on the preselected address fields.

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24. (ONCE AMENDED) A method of routing according to Claim 19, and further comprising the step of generating the start-of-packet interrupt to a communications processor of the network device when the data received within the FIFO receive memory has reached a watermark value.

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27. (ONCE AMENDED) A system for routing network-based data arranged in frames comprising:

a FIFO receive memory of a network device for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a host processor;

a shared system memory that exists between the network device and host processor for receiving data, including the preselected address fields, from the FIFO receive memory;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to the shared system memory; and

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address fields to be

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analyzed by the host processor after receiving a start-of-packet interrupt.

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31. (ONCE AMENDED) A system according to Claim 27, wherein said FIFO receive memory has a watermark value, and means for issuing the start-of-packet interrupt to the communications processor when the watermark value is reached.

32. (ONCE AMENDED) A system for routing network-based data arranged in frames comprising:

a host processor for analyzing transferred bursts of data and initiating an address and lookup algorithm for dispatching a frame to a desired destination;

a shared memory for receiving data, including any preselected address fields; and

a network device having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the receive memory to the shared system memory; and

a communications processor for selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor after receiving a start-of-packet interrupt.

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B10 36. (TWICE AMENDED) A system according to Claim 32, wherein said receive memory has a watermark setting at which the port issues the start-of-packet interrupt to the communications processor.

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B11 38. (ONCE AMENDED) A network controller having:  
a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;  
a direct memory access unit for transferring a burst of data from the FIFO receive memory to an external system memory jointly shared with a host; and  
a communications processor for selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor after receiving a start-of-packet interrupt.

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B12 42. (ONCE AMENDED) A network controller according to Claim 38, wherein said receive memory has a watermark setting at which the port issues the start-of-packet interrupt to the communications processor.

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Please add new Claims 43, 44 and 45 as follows:

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B13 43. A system for routing network-based data arranged in frames comprising:  
a FIFO receive memory of a network device for receiving at least a first portion of a frame, wherein the

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first portion of the frame includes data having preselected address fields;

- a host processor;

- a shared system memory that exists between the network device and host processor for receiving data, including the preselected address fields, from the FIFO receive memory;

- a direct memory access unit for transferring a burst of data from the FIFO receive memory to the shared system memory;

- a communications processor for selecting the amount of data to be transferred from the FIFO receive memory to the shared system memory based on the desired address fields to be analyzed by the host processor; and

- an interrupt bus connected between the FIFO receive memory and communications processor, wherein said FIFO receive memory includes an interrupt generator for generating an interrupt to the communications processor along the bus.

44. A system for routing network-based data arranged in frames comprising:

- a host processor for analyzing transferred bursts of data and initiating an address and lookup algorithm for dispatching a frame to a desired destination;

- a shared memory for receiving data, including any preselected address fields; and

- a network device having:

- a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the

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frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the receive memory to the shared system memory;

a communications processor for selecting the amount of data to be transferred from the receive memory based on the desired address fields to be analyzed by the host processor; and

an interrupt bus connected between the FIFO receive memory and communications processor, wherein said ports include an interrupt generator for generating an interrupt to the communications processor along the bus.

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45. A network controller having:

a plurality of ports, each port including a FIFO receive memory for receiving at least a first portion of a frame, wherein the first portion of the frame includes data having preselected address fields;

a direct memory access unit for transferring a burst of data from the FIFO receive memory to an external system memory jointly shared with a host;

a communications processor for selecting the amount of data to be transferred from the FIFO receive memory based on the desired address fields to be analyzed by a host processor; and

an interrupt bus connected between the FIFO receive memory and communications processor, wherein said ports